UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,467	09/30/2003	Eric J. Strang	231752US6YA	2006

22850 7590 10/10/2006

C. IRVIN MCCLELLAND
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
SAXENA, AKASH	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 10/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/673,467	STRANG, ERIC J.	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-61* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/6/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claim(s) 1-61 has/have been presented for examination based on amendment filed on 6th July 2006.
2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6th July 2006 has been entered.
3. Claim(s) 1, 55 and 58 are amended.
4. Claim(s) 59-61 are new claim(s) added with this amendment.
5. The arguments submitted by the applicant have been fully considered. Claims 1-61 remain rejected. The examiner's response is as follows.

Response to Applicant's Remarks for 35 U.S.C. § 103

6. **Claims 1-21, 23, 25-48, 50 and 52-58 were rejected under 35 U.S.C. 103(a) as being unpatentable over Sonderman, in view of Chen, further in view of Jain.**

Regarding Claim 1-21, 23, 25-48, 50 and 52-58

First applicant has overlooked the fact that this rejection is made with combination of Sonderman-Chen-Jain and not just Sonderman-Jain. Therefore addressing that teaching of Sonderman-Jain alone is improper.

Applicant has argued that

> First, Sonderman et al fail to disclose or suggest a first principles physical model including a set of computer-encoded differential equations or performing first principles simulation for the actual process being performed...In the present case, there appears to be disagreement between the Applicant and the examiner as to whether or not Sonderman et al discloses or suggests the claimed first principles physical model by their disclosure of a device physics model, process model, and an equipment model.

Applicant submits the article "1999 Casting Simulation Software Survey" (Referred to as Midea reference hereafter) as identifying three types of simulations, namely, Empirical, Semi Empirical, and Physics based first principle programs that require complex mathematical and accurate material thermo physical data. This article is used to distinguish the current application from the prior art and further defining the first principle simulation as not the "empirical" or "semi empirical" simulation but "Physics based first principles" simulation.

Examiner asserts that Sonderman and Jain reference provides "Physics based first principles" simulation as disclosed in the submitted article. The reason is set as forth.

Midea teaches first principles simulation as:

> In first principles programs, complex physical relationships and equations are used along with detailed material physical data. The problem must be broken into small calculations via either a finite differencing method or a finite element method. This allows for calculations profile process changes as a function of time.

Using the mold filling example Midea states:

> Mold filling can be predicted using a first principles program. An approach is to employ Navier-stokes flow equations with a two-equation turbulence model. This approach accounts for all relevant flow characteristics (such ms viscosity, friction, Reynold's Number, etc.) in all spatial degrees of freedom. Continuity and the conservation of momentum and energy equations form the basis of these algorithms. This approach is accurate and has been time-tested in the aerospace industry for decades.

As seen above Maeda reference teaches first principles program using complex equations and finite difference methods and as example shows use of Navier-stokes flow equations.

Jain also teaches first principle simulation using complex physical relationships like Navier-stokes flow equations, Maxwells equations for electromagnetic effect. Helmhotlz's Equation for resonant structures, Poisson's equation for steady state temperature and Schroedinger equation for particles in potential field, to name a few used to model various simulations (Jain: Pg. 367-368 Section "Governing Rationale" Sub-Section A. Governing Equations; types of simulation that may cover the three models disclosed by Sonderman).

Further, Jain teaches the first principles simulation, similar to Maeda, because it uses the finite differencing method (Jain: Pg. 368-370 Section "Governing Rationale" Sub-Sections "Finite Difference Method" "Details of Finite Difference Method").

Hence Jain does not fall under the simple empirical or semi-empirical models as described by Maeda but under the "Physics based first principles" of Maeda.

Further, Jain use of the Mathematic Physical Engine (MPE) to simulate semiconductor wafers (Jain Abstract) where at least the fluid flow simulation, thermal flow simulation, diffusion process simulation, chemical Ion exchange simulation, vibration simulation, magnetic simulation and electromagnetic simulation can be applied to the Sonderman's device physics model, process model, and an equipment model.

Secondly, Sonderman does not disclose use of tables of experimental results, rules and physical and guidelines and physical and algebraic equations to model physical process instead teaches cascading complex computation of values based on changes from one model to another (Sonderman: Col.6 Lines 1-16). This indicates that these models cannot be empirical or semi empirical models alone. Sonderman further indicates presence of detailed material physical data (as indicated by from Maeda above) in device physics model where the chemical reactions are modeled with oxide growth emulation (Sonderman: Col.5 Lines 48-55).

Therefore examiner disagrees that Sonderman-Jain combination does not teach the first principles simulation model.

Further, Applicant also points out that the Sonderman discloses statistical response function as denoted by equations 1 & 2 on Col.9.

Examiner agrees with the applicant, however this is not related to the simulation. The Fig.8 being referred to shows a simple feedback process control model of any system (semiconductor manufacturing system here) and not the simulation system. The input Xti to the actual semiconductor manufacturing system takes into account

this statistical feedback as well as simulation (which is based on the actual runs of the semiconductor wafer Si - and not statistical runs). Col.9 Lines 46-51 States:

> The new control inputs, X.sub.Ti, are generally based upon a plurality of factors, such as simulation data, output requirements, product performance requirements, process recipe settings based on a plurality of processing tool 120 operating scenarios, and the like.

Indicating that simulation data is only one of the inputs to the actual semiconductor manufacturing system represented by Fig. 8 & Col.9. Therefore applicant's argument that simulation is based on the statistical response function is unfounded.

Applicant argues that:

> Another question with regard to the first point is whether Sonderman et al disclose providing simulation results for an actual process being performed.

Examiner is unclear if the applicant intentions are to argue temporal sequence between the simulation and actual process being performed. It seems that applicant intends to perform the simulation in parallel with the actual processing that is being performed. If this is the intention, the claim limitation stating, "***using the first principle simulation result to facilitate the actual process being performed by semiconductor processing tool***", ***contradicts*** *the intentions* as clearly the simulation results are used as input to the semiconductor processing performing actual processing.

As stated above Sonderman clearly disclose providing simulation results for an actual process being performed (Sonderman: Col.9 Lines 46-51 States).

Further to point out the difference that Sonderman is not providing simulation results for an actual process being performed applicant has pointed out to Col. 5-7.

Regarding Col.6 Lines 35-47: Applicant has noted that simulation is performed and then the simulation data is passed on the process control. Also noted process control is based on the pre-existing simulation. However, examiner asserts that applicant is providing the arguments in support of the prior art teaching the claimed invention as simulation is performed in the step of "performing first principle simulation ..." and then the results are applied the to actual processing in the step of "using the first principle simulation result to facilitate the actual processing...".

If the intention is that first simulation is not for the process being performed, Sonderman teaches in Col.3 Lines 56-63:

> The process control environment 180 controls the operations of the manufacturing environment 170. In one embodiment, the process control environment comprises an APC framework. The process control environment 180 can receive data from the manufacturing environment 170 and the simulation environment 210 and make appropriate changes to manufacturing control parameters to affect the operations of the manufacturing environment 170.

Further Sonderman states Col.7 Lines 4-7 states:

> Using the validated models, the simulation environment 210 can emulate the operations of an actual process control environment 180 that is integrated with a manufacturing environment 170.

Regarding Col.6 Lines 64-Col.7 Line 7: Applicant presumes that the model validation is based on the historical process data. Examiner respectfully disagrees, Sonderman states that the model validation is defined as **integration** of the "device physics model 310, the process model 320, and the equipment model 330, into a single manufacturing unit that is controlled by the simulator 340." Please see Col.6 Line 67-Col.7 Line 4. If one would infer any other form of validation, although not stated by Sonderman, Jain teaches model validation/verification using the first principle simulation MPE methodology (Jain: Pg.367 "Significance" point 1).

Regarding Col.7 Lines 8-20: Applicant has noted that Sonderman does not perform simulation of the actual manufacturing process; otherwise he would not have stated that "*as if* actual manufacturing process were being performed".

Examiner respectfully disagrees with applicant again, as Sonderman ***is*** performing the *simulation of a manufacturing process* ***not*** *an actual manufacturing process.* Therefore the word "as if" makes sense. Further in light of the claim limitations being contradictory to what is being argued. Sonderman is running simulation based on the same input as would be provided to the actual manufacturing process.

Examiner disagrees for the reasons above that Sonderman does not teach away from the claimed invention.

Applicant argues the second point

> Second, the combination of Sonderman et al and Jain et al fail to produce the claimed invention and is improper.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Sonderman and Jain combined teach the first principle model simulation. Sonderman teaches the device physics model, process model, and an equipment model but limits the details of models to be based on the physical attributes (Col.5 Lines 47—Col.6 Line 16) where change in one is further affects the other. Such a connection is hard to model empirically or even semi empirically as the number of possibilities would be infinite. Jain's reference is used for first principles based

modeling technique using the Mathematical Physical Engine (MPE) and does not need wafer based implementation for it be enabled for simulation purposes as presented in the Sonderman. Sonderman already provides Modeling and simulation facilities. Applicant's argument regarding establishing a prima facie case of obviousness are considered and are found to be unpersuasive.

Applicant further states that Jain's work is better understood in light of Kee patent. Examiner would like to point out Kee reference may have been used by another examiner for enablement, however is not part of the prior art used in this rejection. Jain and Kee are not co-inventors on either of the Kee or Jain references respectively and Examiner finds the arguments moot in view of current rejection.

Response to Applicant's Remarks for 35 U.S.C. § 112¶ 2nd

7. Claim 1-58 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 1

Examiner withdraws the rejection to claims 1-58 based on the argument that the limitation argued (physical & chemical properties of the semiconductor processing tool) are broad not indefinite.

Response to Applicant's Remarks for 35 U.S.C. § 101

8. Applicant arguments relating to Ex parte Lundgren are not germane to the arguments made here as no rejection was made under "technological arts" test. Further, interim guidelines may leave the issue of tangibility to open to comments as

indicated by applicant, however the current office policy is to reject all claims directed to "transmission media" as an embodiment of the invention as non-statutory. The current 35 USC 101 rejection is maintained.

Response to Applicant's Remarks for Double Patenting

9. Applicant's arguments relating to filing a terminal disclaimer for applications 10/673,507 are considered and double patenting rejection is maintained until a terminal disclaimer is filed.

Claim Rejections - 35 USC § 112¶1st

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

10. Claim 1-61 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. Exact details of what basic physical and chemical attribute of the semiconductor processing tool are used to construct a first principle simulation model which is critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

Applicant has argued that the meaning of the basic physical and chemical attribute of the semiconductor-processing tool is discernable to one of ordinary skill in the art. Although, teaching in the Maeda reference is present in exemplary format of molding tool, it is not there for a semiconductor-processing tool and does showing the physical and chemical attribute of the semiconductor-processing tool. Further, neither claim not the disclosure presents physical and chemical attribute of the semiconductor-processing tool in form of the first principles models. Examiner requests the applicant to provide an exact support in disclosure for such attributes in the model.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

11. Claims 58 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 58 discloses "computer readable medium" which is defined in the specification (Pg.32-33 [00103] Line1-9) to include tangible items ("non volatile media" and "volatile media") and items that are non-tangible ("transmission media"). Therefore the claim as whole is not directed towards a tangible medium. One possible suggested way to overcome this rejection is to replace "computer readable medium" with "non volatile media" and "volatile media". Transmission media (Carrier wave) is understood be non-statutory and rejected under current office practice.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claim 1 provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/673,507 (updated 9/19/06).

Application No. 10/673,467	Application No. 10/673,507
A method of controlling a process performed by a semiconductor processing tool, comprising:	A method of controlling a process performed by a semiconductor processing tool, comprising:
inputting data relating to a process performed by the semiconductor processing tool;	inputting data relating to a process performed by the semiconductor processing tool;
inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attributes of the semiconductor processing tool;	inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool;;
performing first principles simulation *for the actual process being performed* **using the input data** and the physical model to provide a first principles simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed;	performing first principles simulation *for the actual process being performed* using the physical model to provide a first principles simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed; and

using the first principles simulation result to build an empirical model; and	
selecting at least one of the first principles simulation result and the empirical model to control the process performed by the semiconductor processing tool.	and using the first principles simulation result to control the *actual* process performed by the semiconductor processing tool.

Although the conflicting claims are not identical, they are not patentably distinct from each other because the step of building an empirical model is inherent with the physical model. Further, both the specifications are identical in implementation and there is no difference in the implementation of the two models. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented. Further the step of "selecting" which not present in the 10/673,507, is evident in the using the result to control the actual process.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. Claims 1-21, 23, 25-48, 50 and 52-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of U.S. Patent No. 5,719,796 issued to Vincent M.C. Chen (Chen hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter).

Regarding Claim 1

Sonderman teaches a method to controlling a process performed by a semiconductor-processing tool (Sonderman: Summary, at least in Col.2 Lines 10-17;Col.3 Lines 45-49) by inputting *process* data relating to *an actual* process *being* performed by the semiconductor-processing tool (Sonderman: at least in Col.3 Lines 50-67; *Col.7 Lines 8-20*). Further, Sonderman teaches inputting the first principle physical model relating to the semiconductor-processing tool *describing at least one of a basic physical or chemical attributes* (Sonderman: at least in Col.5 Lines 11-17; 49-67) as device physics model, a process model and an equipment model. Further, Sonderman teaches performing first principle simulation *for the actual process being performed (Sonderman: Col.7 Lines 4-7; Col.3 Lines 56-63)* using the input data and the physical model to provide simulation results for the process performed by the semiconductor–processing tool (Sonderman: at least in Col.5-7). Further, Sonderman teaches using the first principle simulation results to control the *actual* process *being* performed by the semiconductor-processing tool (Sonderman: at least in Col.4 Lines 48-64; Fig.1-8; Col.2 Lines 10-17).

Sonderman does not explicitly teach building an empirical model and using the first principle simulation results along with the empirical model to control the process performed by the semiconductor-processing tool. Empirical model & library as understood from the specification ([0078]) is the database of the simulation results, which provides "statistically sufficient sample of the parameter space".

Chen teaches creating an empirical model as disclosed in the specification as a statistical model built based on run-to-run or batch-to-batch results and using the results to control the process performed by the semiconductor-processing tool as well as to the next simulation step (Chen: Col.3 Lines 12-47; Col.6 Lines 34-67).

Sonderman and Chen do not teach first principle model including a set of computer encoded differential equations.

Jain teaches computer encoded differential equations using MPE engine, which can be applied to wafer processing (Jain: Abstract). Jain also teaches dedicated and wafer level implementation of MPE engine to provide enhanced performance (Jain: Pg. 372 Section V Dedicated MPE).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Chen to Sonderman. The motivation to combine would have been that Chen and Sonderman both are analogous art concerned with simulating the semiconductor fabrication process and providing the best control parameters to the actual semiconductor-processing tool (Chen: at least in Col.3 Lines 19-23).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Jain to Sonderman to solve differential equation for the semiconductor processing tool. Sonderman teaches building various models, which work in real-time feedback control simulating actual semiconductor modeling process (Sonderman: Fig.1; *Col.7 Lines 8-20*), while Jain makes possible by providing model-solving capacity in real time when differential equations are present in the model (like thermal patterns in semiconductor wafer model) (Jain: Abstract).

Regarding Claim 2

Sonderman teaches directly inputting the *process* data relating to the *actual* process *being* performed by the semiconductor-processing tool from at least one of physical sensor (eg. Scatterometry data, overlay data, dimensional data) and a metrology tool physically mounted on the semiconductor-processing tool (Sonderman: at least in Col.4 Lines 31-48; Col.4-8; Fig.1, 7; *Col.7 Lines 8-20*).

Regarding Claims 3-5

Sonderman teaches indirectly inputting the *process* data relating to the *actual* process performed by the semiconductor-processing tool from one of the manual input devices and a database as manual fashion data retrieval and automatic data retrieval; inputting data recorded from the previous run; inputting the data set by a simulation operator (Sonderman: at least in Fig.1-3 Col.1; Col.4-7; Col.7 Lines 8-20).

Regarding Claims 6-9

Sonderman teaches inputting *process* data relating to at least one of the physical characteristics of the semiconductor-processing tool and semiconductor tool environment, data relating to at east on of the characteristics and a result of a process performed by the semiconductor processing tool; inputting a spatially resolved model (as modified models) of the geometry of the semiconductor processing tool; inputting fundamental equations necessary to perform first principle simulation for the desired simulation result (Sonderman: at least in Col.5 Lines 10-18; Col.6 Lines 48-63; Col.9 (equations); Col.5-9; Fig 1-3; *Col.7 Lines 8-20*). Sonderman and Jain teach inputting fundamental equations *as the set of computer encoded differential equations* (Sonderman: Col.9 (equations); Jain: Pg. 372 Section V Dedicated MPE, Abstract).

Regarding Claim 10

Sonderman teaches performing interaction concurrently between the simulation environment (first principle simulation) and the semiconductor-processing tool (Sonderman: Fig.2; Col.4 Lines 48-63).

Regarding Claims 11-13

Sonderman teaches performing first principle simulation independent of the process performed by the semiconductor-processing tool; inputting data from to set initial & boundary condition on the first simulation model (Sonderman: at least in Col.5-8; Fig.3-4).

Regarding Claim 14

Sonderman teaches using the first principles simulation result comprises using the first principles simulation result to perform at least one of detecting, and classifying a fault in the process performed by the semiconductor-processing tool (Sonderman: at least in Col.5 Line 56 – Col.6 Line 24).

Regarding Claims 15-19

Sonderman teaches using a network of interconnected resources to perform at least one of the process steps recited in claim 1; using code parallelization among interconnected computational resources to share the computational load of the first principle simulation; sharing simulation information among the interconnected resources to facilitate a process by the semiconductor-processing tool; sharing simulation results among the interconnected resources to reduce redundant execution of substantially similar first principle simulation by different resources; sharing information comprising model changes among the interconnected resources to reduce the redundant refinements of first simulation by different resources (Sonderman: Fig.1-3, computer code software is described in Col.9 Lines 58 onward; Col.5-8).

Regarding Claims 20-21

Sonderman teaches remote access to computational and storage resources (Sonderman: Col.9 Line 58-Col.10 Line 31) where in wide area network is art inherent.

Regarding Claim 23

Sonderman teaches first principle simulation controlling at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposition system, a rapid thermal processing system for thermal annealing, and a batch diffusion furnace (Sonderman: at least in Col 4 Lines 18-31; Col.3 Lines 45-49).

Regarding Claim 25

Sonderman teaches inputting various parameters relating to etching, deposition etc. (Sonderman: at least in Col.5 Lines 56-67)

Regarding Claim 26

Sonderman teaches inputting physical geometric data as parameters for the equipment model where the equipment could be at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposition system, a rapid thermal processing system for thermal annealing, and a batch diffusion furnace (Sonderman: Col.5 Lines 56-67).

Regarding Claim 27

Sonderman teaches first principles simulation result controlling the semiconductor processing tool by using model output to adjust said process performed by the semiconductor processing tool (Sonderman: Col.4 Lines 48-64; Fig.1-2).

Regarding Claim 28-48

System claims 28-48 disclose similar limitations as claims 1-21 and are rejected for the same reasons as claims 1-21 respectively.

Regarding Claim 50, 52-54

System claims 50 & 52-54 disclose similar limitations as claims 23 & 25-27 and are rejected for the same reasons as claims 23 & 25-27 respectively.

Regarding Claim 55

System claim 55 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 56 & 57

System claims 56 & 57 disclose similar limitations as claims 16 & 17 and are rejected for the same reasons as claims 16 & 17 respectively.

Regarding Claim 58

Article of Manufacture (computer program) claim 58 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1.

Regarding Claims 59-61(New Claims)

Jain teaches use of Navier Stokes and other known simulation solutions (reuse) for solving various simulation problems as initial condition (Jain: Pg. 367-368 Section "Governing Rationale" Sub-Section A. Governing Equations). Sonderman also teaches initializing the models with input data (Sonderman: Col.7 Lines 8-20).

4. **Claims 22 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of U.S. Patent No. 5,719,796 issued to Vincent M.C. Chen (Chen hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter), further in view of IEEE article "Heat Analysis on Insulated Metal Substrates" by Naomi Yunemura et al (Yunemura hereafter).**

Regarding Claim 22

Teachings of *Sonderman, Chen and Jain* are disclosed in claim 1 rejection above. Sonderman also teaches that the first principle simulation models the equipment conditions, thereby modeling temperature response and pressure response during various processes (Sonderman: at least in Col.5 Lines 62-67).

Sonderman, Chen and Jain does not teach explicitly that such temperature and pressure modeling is done using ANSYS computer code. *However, Jain teaches SIMD based processing to solve the computer-encoded differential equations (Jain: Pg. 370 Section III Parallel architectures for solving PDE).*

Yunemura teaches that heat simulation modeling can be performed using ANSYS computer code (Yunemura: Pg. 1407 Section 1) on a silicon chip.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Yunemura to Sonderman, Chen and Jain to create a equipment model as disclosed by Sonderman. The motivation to combine would have been that Yunemura teaches heat modeling on a

silicon chip affecting the thermal conductivity (Yunemura: Pg.1407 Section 2) based on various thicknesses and Sonderman is solving the same issue for the equipment model that for example model the equipment for depositing the various layers and affects on heat and pressure. ANSYS is known in art to be used as thermal & pressure modeling tool based on finite element analysis. Yunemura's teaching thereby facilitates computer-encoded differential equations solving which is considered to be prime issue by Jain (Jain: See Section III, Networking and Dedicated MPE's for solving the computer-encoded differential equations).

Regarding Claim 49

System claim 49 discloses similar limitations as claim 22 and is rejected for the same reasons as claim 22.

5. **Claims 24 & 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of U.S. Patent No. 5,719,796 issued to Vincent M.C. Chen (Chen hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter), further in view of U.S. Patent No. 6,812,045 issued to Mehrdad Nikoonahad (Nikoonahad hereafter).**

Regarding Claim 24

Teachings of *Sonderman, Chen and Jain* are disclosed in claim 1 rejection above. Sonderman provides examples of the processing tool as etch and photolithography tools (Col.4 Lines 26-31) *but does not explicitly disclose chemical vapor and physical vapor deposition system.* Chen teaches fabrication equipment as Chemical Vapor Deposition (CVD) system (Col.5 Lines 1-5) but does not teach physical vapor deposition system. *Jain is moot on such teachings.*

Nikoonahad teaches deposition tools to include chemical vapor and physical vapor deposition system (Nikoonahad: Col.24 Lines 3-49).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Nikoonahad to *Sonderman, Chen and Jain.* The motivation to combine would have been that Nikoonahad and Sonderman-Chen are analogous art and both are modeling the semiconductor processing and providing feedback to the semiconductor processing

tool (Sonderman: Abstract; Nikoonahad: Col.3; Col.93 Lines 20-35; Chen: Summary).

Regarding Claim 51

System claim 51 discloses similar limitations as claim 24 and is rejected for the same reasons as claim 24.

Conclusion

13. All claims are rejected.

14. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 9:30 - 6:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Akash Saxena
Patent Examiner, GAU 2128
(571) 272-8351
Tuesday, September 19, 2006

Kamini S. Shah
Supervisory Patent Examiner, GAU 2128
Structural Design, Modeling, Simulation and Emulation